CLAIMS

1. A photodetector, having a photosensitive region, in which pixels are arrayed two-dimensionally, and being used with a light source that illuminates light onto an object, wherein

a single pixel is arranged by adjacently positioning on the same plane a plurality of photosensitive portions, each outputting a current that is in accordance with an intensity of light incident thereon and,

in each plurality of pixels that are aligned in a first direction of the two-dimensional array, one photosensitive portion among the plurality of photosensitive portions making up each corresponding pixel is electrically connected to the same photosensitive portion of each of the other corresponding pixels and,

in each plurality of pixels that are aligned in a second direction of the two-dimensional array, another photosensitive portion among the plurality of photosensitive portions making up each corresponding pixel is electrically connected to the same photosensitive portion of each of the other corresponding pixels,

the photodetector comprising: a first signal processing circuit, detecting a luminance profile in the second direction based on differences between outputs, corresponding to charges accumulated in first groups of the photosensitive portions that are electrically connected across the pluralities of pixels aligned in the first direction over a first period wherein the light is illuminated onto the object by the light source, and outputs, corresponding to charges accumulated in the first groups of the photosensitive portions over a second period wherein the light is not illuminated onto the object by the light source; and

a second signal processing circuit, detecting a luminance profile in the first direction based on differences between outputs, corresponding to charges accumulated in second groups of the photosensitive portions that are electrically connected across the pluralities of pixels aligned in the second direction over the first period, and outputs, corresponding to charges accumulated in the second groups of the photosensitive portions over the second period.

2. The photodetector according to Claim 1, wherein the first signal processing circuit comprises:

a first shift register for successively reading, in the second direction, the electric currents from the first groups of the photosensitive portions

a first integrating circuit, successively inputting the electric currents from the respective first groups of the photosensitive portions that are read successively by the first shift register and converting and outputting the electric currents into and as a voltage;

a first CDS circuit, outputting a voltage corresponding to the variation amount of the voltage from the first integrating circuit;

a first A/D conversion circuit, converting the voltage from the first CDS circuit into digital values and outputting the digital values; and

a first difference operational circuit, determining, based on the digital values output from the first A/D conversion circuit, differences between digital values corresponding to the first period and digital values corresponding to the second period; and

the second signal processing circuit comprises:

a second shift register for successively reading, in the first direction, the electric currents from the second groups of the photosensitive portions;

a second integrating circuit, successively inputting the electric currents from the respective second groups of the photosensitive portions that are read successively by the second shift register and converting and outputting the electric currents into and as a voltage;

a second CDS circuit, outputting a voltage corresponding to the variation amount of the voltage from the second integrating circuit;

a second A/D conversion circuit, converting the voltage from the second CDS circuit into digital values and outputting the digital values; and

a second difference operational circuit, determining, based on the digital values output from the second A/D conversion circuit, differences between digital values corresponding to the first period and digital values corresponding to the second period.

3. The photodetector according to Claim 2, wherein the first signal processing circuit further comprises: a first digital memory, disposed between the first A/D conversion circuit and the first difference operational circuit and storing the digital values corresponding to the first period and the digital values corresponding to the second period and outputting the stored digital values to the first difference operational circuit; and

the second signal processing circuit further comprises: a second digital memory, disposed between the second A/D conversion circuit and the second difference operational circuit and storing the digital

values corresponding to the first period and the digital values corresponding to the second period and outputting the stored digital values to the second difference operational circuit.

4. The photodetector according to Claim 1, wherein the first signal processing circuit comprises:

first integrating circuits, provided in correspondence to the first groups of the photosensitive portions and each converting and outputting the electric currents from the corresponding first group of the photosensitive portions into and as a voltage;

first CDS circuits, disposed in correspondence to the first integrating circuits and each in turn comprising a first coupling capacitance element and a first amplifier, disposed in that order between an output terminal and an input terminal that inputs the voltage from the corresponding first integrating circuit, a first integrating capacitance element, disposed in parallel between the input and the output of the first amplifier, and a first switching element, making charges of an amount corresponding to the variation amount of the voltage be accumulated in the first integrating capacitance element;

second CDS circuits, disposed in correspondence to the first integrating circuits and each in turn comprising a second coupling capacitance element and a second amplifier, disposed in that order between an output terminal and an input terminal that inputs the voltage from the corresponding first integrating circuit, a second integrating capacitance element, having a capacitance value equal to the capacitance value of the first integrating capacitance element and disposed in parallel between the input and the output of the second

amplifier, and a second switching element, making charges of an amount corresponding to the variation amount of the voltage be accumulated in the second integrating capacitance element; and

first difference operational circuits, disposed in correspondence to the first CDS circuits and the second CDS circuits and each determining a difference in the amounts of charges respectively accumulated in the first integrating capacitance element of the corresponding first CDS circuit and the second integrating capacitance element of the corresponding second CDS circuit and outputting a voltage that is in accordance with the difference; and

the second signal processing circuit comprises:

second integrating circuits, provided in correspondence to the second groups of the photosensitive portions and each converting and outputting the electric currents from the second corresponding group of the photosensitive portions as a voltage;

third CDS circuits, disposed in correspondence to the second integrating circuits and each in turn comprising a third coupling capacitance element and a third amplifier, disposed in that order between an output terminal and an input terminal that inputs the voltage from the corresponding second integrating circuit, a third integrating capacitance element, disposed in parallel between the input and the output of the third amplifier, and a third switching element, making charges of an amount corresponding to the variation amount of the voltage be accumulated in the third integrating capacitance element;

fourth CDS circuits, disposed in correspondence to the second integrating circuit and each in turn comprising a fourth coupling

capacitance element and a fourth amplifier, disposed in that order between an output terminal and an input terminal that inputs the voltage from the corresponding second integrating circuit, a fourth integrating capacitance element, having a capacitance value equal to the capacitance value of the fourth integrating capacitance element and disposed in parallel between the input and the output of the fourth amplifier, and a fourth switching element, making charges of an amount corresponding to the variation amount of the voltage be accumulated in the fourth integrating capacitance element; and

second difference operational circuits, disposed in correspondence to the third CDS circuits and the fourth CDS circuits and each determining a difference in the amounts of charges respectively accumulated in the third integrating capacitance element of the corresponding third CDS circuit and the fourth integrating capacitance element of the corresponding fourth CDS circuit and outputting a voltage that is in accordance with the difference.

5. The photodetector according to Claim 4, wherein the first signal processing circuit further comprises:

first sample-and-hold circuits, provided in correspondence to the first difference operational circuits and each holding and then outputting the voltage from the corresponding first difference operational circuit; and

a first A/D conversion circuit, successively inputting the voltages from the respective first sample-and-hold circuits, converting the voltages into digital values, and outputting the digital values; and

the second signal processing circuit further comprises:

second sample-and-hold circuits, provided in correspondence to the second difference operational circuits and each holding and then outputting the voltage from the corresponding second difference operational circuit; and

a second A/D conversion circuit, successively inputting the voltage from the respective second sample-and-hold circuits, converting the voltage into digital values, and outputting the digital values.

6. The photodetector according to Claim 1, wherein the first signal processing circuit comprises:

first charge accumulation circuits, provided in correspondence to the respective first groups of the photosensitive portions and each comprising a first capacitance element and a second capacitance element, disposed in parallel between an output terminal and an input terminal that inputs the electric currents from the corresponding first group of the photosensitive portions, and accumulating charges in the first capacitance element in accordance with the electric currents corresponding to the charges accumulated during the first period in the corresponding first group of the photosensitive portions and accumulating charges in the second capacitance element in accordance with the electric currents corresponding to the charges accumulated during the second period in the corresponding first group of the photosensitive portions; and

a first difference operational circuit, determining the differences between the charge amounts accumulated respectively in the first capacitance elements and the second capacitance elements of the first charge accumulation circuits and outputting a voltage that is in

accordance with the differences; and

the second signal processing circuit comprises: second charge accumulation circuits, provided in correspondence to the respective second groups of the photosensitive portions and each comprising a third capacitance element and a fourth capacitance element, disposed in parallel between an output terminal and an input terminal that inputs the electric currents from the corresponding second group of the photosensitive portions, and accumulating charges in the third capacitance element in accordance with the electric currents corresponding to the charges accumulated during the first period in the corresponding second group of the photosensitive portions and accumulating charges in the fourth capacitance element in accordance with the electric currents corresponding to the charges accumulated during the second period in the corresponding second group of the photosensitive portions; and

a second difference operational circuit, determining the differences between the charge amounts accumulated respectively in the third capacitance elements and the fourth capacitance elements of the second charge accumulation circuits and outputting a voltage that is in accordance with the differences.

7. The photodetector according to Claim 6, wherein the first signal processing circuit furthermore comprises:

a first integrating circuit, successively inputting, from the first capacitance elements and the second capacitance elements, electric currents corresponding to the charges accumulated in the corresponding first capacitance elements and second capacitance elements and

converting the electric currents into a voltage and outputting the voltage to the first difference operational circuit; and

a first A/D conversion circuit, successively inputting the voltage from the first difference operational circuit, converting the voltage into digital values, and outputting the digital values; and

the second signal processing circuit furthermore comprises:

a second integrating circuit, successively inputting, from the third capacitance elements and the fourth capacitance elements, electric currents corresponding to the charges accumulated in the corresponding third capacitance elements and fourth capacitance elements and converting the electric currents into a voltage and outputting the voltage to the second difference operational circuit; and

a second A/D conversion circuit, successively inputting the voltage from the second difference operational circuit, converting the voltage into digital values, and outputting the digital values.

8. A photodetector, having a photosensitive region, in which pixels are arrayed two-dimensionally, and being used with a light source that illuminates light onto an object, wherein

a single pixel is arranged by adjacently positioning on the same plane a plurality of photosensitive portions, each outputting a current that is in accordance with an intensity of light incident thereon and,

in each plurality of pixels that are aligned in a first direction of the two-dimensional array, one photosensitive portion among the plurality of photosensitive portions making up each corresponding pixel is electrically connected to the same photosensitive portion of each of the other corresponding pixels and,

in each plurality of pixels that are aligned in a second direction of the two-dimensional array, another photosensitive portion among the plurality of photosensitive portions making up each corresponding pixel is electrically connected to the same photosensitive portion of each of the other corresponding pixels,

the photodetector comprising: first eliminating circuits, being provided in correspondence to the respective first groups of the photosensitive portions, which are electrically connected across each the plurality of pixels aligned in the first direction, and each eliminating a electric current, which is output from the corresponding first group of the photosensitive portions in a second period wherein the light is not illuminated onto the object by the light source, from a electric current, which is output from the corresponding first group of the photosensitive portions in a first period wherein the light is illuminated onto the object by the light source, and outputting the electric current resulting from the elimination;

first integrating circuits, being provided in correspondence to the first eliminating circuits and each accumulating charges in accordance with the electric current from the corresponding first eliminating circuit and outputting a voltage that is in accordance with the amount of the accumulated charges;

second eliminating circuits, being provided in correspondence to the respective second groups of the photosensitive portions, which are electrically connected across each the plurality of pixels aligned in the second direction, and each eliminating a electric current, which is output from the corresponding second group of the photosensitive portions in

the second period, from a electric current, which is output from the corresponding second group of the photosensitive portions in the first period, and outputting the electric current resulting from the elimination; and

second integrating circuits, being provided in correspondence to the second eliminating circuits and each accumulating charges in accordance with the electric current from the corresponding second eliminating circuit and outputting a voltage that is in accordance with the amount of the accumulated charges.

9. The photodetector according to Claim 8, wherein each of the first eliminating circuit comprises:

a first MOS transistor, having a source terminal connected to the corresponding first group of the photosensitive portions and a drain terminal that is grounded;

a first capacitance element, having one terminal connected to a gate terminal of the first MOS transistor and another terminal that is grounded; and

a first switching element, having one terminal connected to the gate terminal of the first MOS transistor and another terminal connected to the output of the corresponding first integrating circuit; and

each second eliminating circuit comprises:

a second MOS transistor, having a source terminal connected to the corresponding second group of the photosensitive portions and a drain terminal that is grounded;

a second capacitance element, having one terminal connected to a gate terminal of the second MOS transistor and another terminal that

is grounded; and

a second switching element, having one terminal connected to the gate terminal of the second MOS transistor and another terminal connected to the output of the corresponding second integrating circuit.

10. The photodetector according to Claim 8, further comprising:

first difference operational circuits, provided in correspondence to the first integrating circuits and each holding, from among the voltages from the corresponding first integrating circuit, the voltage corresponding to the second period and outputting a voltage that is in accordance with the difference with respect to the voltage, which, among the voltages from the corresponding first integrating circuit, corresponds to the first period;

first sample-and-hold circuits, provided in correspondence to the first difference operational circuits and each holding and outputting the voltage from the corresponding first difference operational circuit;

a first A/D conversion circuit, successively inputting the voltages from the respective first sample-and-hold circuits, converting the voltages into digital values, and outputting the digital values;

second difference operational circuits, provided in correspondence to the second integrating circuits and each holding, from among the voltages from the corresponding second integrating circuit, the voltage corresponding to the second period and outputting a voltage that is in accordance with the difference with respect to the voltage, which, among the voltages from the corresponding second integrating circuit, corresponds to the first period;

second sample-and-hold circuits, provided in correspondence to

the second difference operational circuits and each holding and then outputting the voltage from the corresponding second difference operational circuit; and

a second A/D conversion circuit, successively inputting the voltages from the respective second sample-and-hold circuits, converting the voltages into digital values, and outputting the digital values.